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(54) Title of Invention: Device for segmented transmission of television signals

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Specification

1. Title of Invention

Device for segmented transmission of television signals

2. Claims

A device for the segmented transmission of television signals which, with respect to a device for the segmented transmission of television signals which segments television signals at the transmission end into 1 - n digital signals (n ≥2), transmits these in parallel through 1 - n transmission paths, and combines the received 1 - n segmented signals to reconstruct the original television signal at the receiving end, is characterised in that

the transmission end is provided with a synchronous signal selector circuit (13) which transmits the television signals divided into blocks of field units, line units or pixel units,

the receiving end being provided with a signal synthesiser means (14) which, where omissions or errors have occurred in part of the digital signals being segmentally transmitted in the intervening transmission paths, the limit for error correction decoding of the signal having been exceeded, substitutes said segmented signal with another normal segmented signal, and a means (15) which samples a clock from a normal segmented signal.

3. Detailed Description

(Summary)

In a method for the segmented transmission of television signals which segments television signals at the transmission end into 1 - n digital signals (n ≥2), transmits these in parallel through 1 - n transmission paths, and combines the

received 1 - n segmented signals to reconstruct the original television signal at the receiving end,

sending from the transmitting end television signals that have been segmented into block units which use the characteristics of a television signal such as field units, line units and pixel units,

where an omission or error occurs in part of a data signal in transmission paths 1 - n, the provision at the receiving end of a function which determines said signals, together with the rejection of segmented signals determined as having an omission or error, using in their place segmented signals with adjacent fields, adjacent lines or adjacent pixels that have a close correspondence in terms of the characteristics of the picture composition of the television signal,

and additionally in respect of clock sampling from the received signals, the execution of clock sampling from normal segmented signals, avoiding segmented signals that have been determined to have an omission or error,

ensures the restoration of the television image with little deterioration in picture quality, even where omissions or errors occur in part of the data signals sent through 1 - n transmission paths.

(Field of Industrial Use)

The invention relates to an improvement in a device for the segmented transmission of television signals which, in a device for the segmented transmission of television signals which segments television signals at the transmission end into 1 - n digital signals ($n \geq 2$), transmits these in parallel through 1 - n transmission paths, and combines the received 1 - n segmented signals to reconstruct the original television signal at the receiving end.

In the field of the digital transmission of television signals, where there are limits to the transmission capacity of the transmission paths (transmission speed) it is common practice as a means of resolving the situation in an economical manner to transmit the original television signal segmentally in a plurality of low-speed digital transmission paths, and then restore the original television signal once more at the receiving end.

It is desirable that there should be a means of maintaining the picture quality of the original image even where encoding errors or omissions occur in part of the segmented signals due to the circumstances of transmission in the transmission process.

(Prior Art)
Fig.2 is a block diagram illustrating the structure of a conventional circuit at the transmitting end, Fig.3 a block diagram illustrating the structure of a conventional circuit at the receiving end, Fig.4 being a time chart showing data signals for the main parts illustrated in Figs 2 and 3, lines (A), (B), (C)... (G) in Fig 4 corresponding respectively to parts keyed as a, b, c.... g in Figs.2 & 3.

Fig.5 is an example of a block diagram showing of the detail of the control signal generator in Fig 2 and in Fig. 3, and Fig.6 is a block diagram showing an example of the detail of the segment selector in Fig.2.

Fig.2 shows an example where there are two segmented signals (n = 2). In the figure,

clock generator circuit 6 is a circuit which supplies the necessary clock signal to each circuit at the transmission end, the repeat frequency of the transmission path clock CL-2 being one half that of the repeat frequency of encoded clock CL-1.

An analog television signal is first input to terminal D of

segment selector 33 via A/D converter 1 and band compression encoder 2.

Segment selector 33 segments the data signal as shown in Fig.4(A) and (B) in accordance with the timing of the control signal supplied from control signal generator circuit 32 to its terminal S, outputting alternately from output terminals A and B.

A more specific description will now be made of this process using examples of control signal generator circuit 32 and the circuit of segment selector 33.

The first example of a circuit for control signal generator circuit 32 is an FF circuit as shown in Fig.5(A) , a control signal having the waveform shown in (B) of the same figure being output from terminal Q at a timing determined by the trigger pulse input to terminal CL. In the structure of a conventional transmission end circuit, a rounded-up signal counted out by counter 31 to one block's worth of data for a specific number of pulses is input as the input trigger pulse, as shown in Fig.2.

The first example of a circuit for segment selector 33 is the circuit shown in Fig.6, 1st and 2nd segmented data signals being alternately output from output terminals A and B by means of a control signal such as that as shown in Fig.5 (B) being input to its terminal S from control signal generator circuit 32.

After respectively passing through segmenting FF circuit 34,35, and having been stored temporarily in buffer memories 41, 42, these segmented data signals are then read out by clock signal CL-2 and subjected to transmission frame structuring/error correction encoding, and output to 1st and 2nd transmission paths as a low speed data signal as shown in Fig.4 (C) and (D).

Next at the receiving end with 1st and 2nd segmented data signals (C) and (D) received from the transmission paths

undergo error correction at receiver 7, and, passing through a transmission frame analysis process, are stored respectively in buffer memories 81, 82, being read out by decoding clock signal CL-1' from clock sampling circuit 12, the input signals to terminals A and B of synthesis selector 93 from synthesis FF circuits 91,92 being respectively signals of odd- or even-numbered blocks repeated twice as shown in Fig.4 (E) and (F).

Counter 94 of synthesiser 9 counts the number of pulses of a single block's worth of the original data signal using the period of decoding clock CL-1', and, as a control signal is now input to terminal S of synthesis selector 93 from control signal generator circuit 95 on the basis of this rounded-up signal, a synthesised signal is output from the output terminal D of synthesis selector 93 as shown in Fig.4(G), the original analog TV signal being restored after passing through band compression restoration and D/A conversion.

In cases where, in general, $n \geq 3$,

for each segmented signal clock

(a) the repeat frequency is 1/n of the repeat frequency of CL-1

(b) the phase delay for the 2^{nd} - n^{th} segmented signal clocks with respect to the 1^{st} segmented signal clock is

2^{nd} segmented signal clock is $2\pi \times (1/n)$
3^{rd} segmented signal clock is $2\pi \times (2/n)$
"
"
"
n^{th} segmented signal clock is $2\pi \times (n-1/n)$

if n pulses are used as the clocks for each transmission path, segmentation and synthesis are possible using a similar means to that described above.

(Problems to be Resolved by the Invention)

However, should errors or omissions occur in even one of the data signals in a transmission path in the intervening 1-n transmission paths, the problem will be that, since the segmented signal is not accurate, severe deterioration will occur in the restored television image, and, should an error occur in the transmission path from which the clock is sampled at the receiving end, it will be very difficult to restore the image.

(Means of Resolving the Problems)

As shown in the block diagram illustrating the principles of the invention in Fig.1, the above problems can be resolved using a device for the segmented transmission of television signals according to the invention, arranged such that before being sent from the transmission end the television signals are segmented into block segments which make use of the characteristics of television signals such as field units, line units, or pixel units, and such that, should an omission or error occur in part of a data signal in transmission paths 1 - n, not only is the receiving end provided with a function which determines said signal, but a normal segmented signal is substituted in place of the segmented signal that has been determined to have an omission or error, and additionally, in respect of clock sampling from the received signals, clock sampling is executed from a normal segmented signal, avoiding segmented signals that have been determined to have an omission or error.

(Action)

Thus, according to the invention,

television signals are not segmented into arbitrary blocks at the transmission end as in prior art, but synchronous signal sampling circuit 13 which samples a fixed synchronous signal

from the television image signal is provided so that they are transmitted having been segmented into block units which make use of the characteristics of television signals such as field units, line units, or pixel units,

and, should an omission or error in the data signal occur in the intervening transmission paths, the receiving end is provided with a function which determines said signals using an error correction limit signal,

and, where an omission or error is determined to have occurred, said segmented signal is not used, but control signal selection circuit 14 is provided at the synthesiser to substitute a segmented signal with an adjacent field, adjacent line or adjacent pixel bearing a close correspondence to the signal as a replacement,

and additionally, in respect of clock sampling from the received signals, received signal selector 15 is provided so that clock sampling is executed using a normal segmented signal, avoiding segmented signals that have been determined to have an omission or error,

thus ensuring the restoration of a television image with little deterioration in picture quality even where omissions or errors occur in part of the data signals sent through the transmission paths.

(Embodiment)

An embodiment will now be described where the segmentation is in field units that have been divided into 2 segments of odd and even groups (n = 2).

In the block diagram illustrating the transmission end circuit structure of an embodiment of the invention shown in Fig.7, band compression encoding unit 2, control signal generator circuit 32, segment selector 33, segment FF circuits 34, 35,

buffer memories 41, 42, transmitter 5 and clock generator circuit 6 are identical circuits to those used in the conventional example shown in Fig.2, A/D converter 1' being provided, in addition to the conventional A/D converter function, with synchronous signal sampling circuit 13 which provides a trigger pulse to control signal generator circuit 32, extracting a synchronous signal (vertical) from the field signal.

Thus odd- and even-numbered fields are transmitted alternately as segmented signals to 1st transmission path and 2nd transmission path from the transmitting end.

In the block diagram illustrating the structure of the circuit at the receiving end of an embodiment of the invention in Fig.8, buffer memories 81, 82, synthesis FF circuits 91, 92, synthesis selector 93, control signal generating circuit 95, band compression encoder 10, D/A converter 11 and clock sampling circuit 12 are all identical circuits to those used in the conventional example shown in Fig.3, but error correction decoding circuits 71', 72' are provided additionally with a detection signal generator function according to the invention, and moreover synchronous signal sampling circuit 96, control signal selection circuit 14, and receiving signal selector 15 are circuits added in accordance with the invention.

The additional functions and circuits will now be described in detail.

The error correction encoding method normally employed is a method which carries out corrections on the basis of an encoding logic at the receiving end in the same way as the BCH encoding system, adding a certain number of correction bits to each block of data signals at the transmission end, the limit for the correction of error being determined by the number of bits of error correction added in this case, and, where this limit is exceeded, has a function which can determine this. (See Data Communications Handbook, Electronic Communications

Congress ed.)

On this basis error correction decoding circuits 71',72' are provided with a discriminating signal generating function which generates the symbol "1" (high-level) as the discriminating signal for error correction when it is possible to correct the error, and the symbol "0" (low-level) when the limit for error correction has been exceeded, so that it is possible to determine the existence of omissions or areas in the received data signal.

When the input data signals of 1st transmission path are normal, synchronous signal sampling circuit 96 of synthesiser unit 9' is a timing pulse sampling circuit for synthesis which distributes 1st and 2nd data signals alternately according to the timing of the (vertical) synchronous signal of this field signal, the sampled pulse being input to control signal generator circuit 95.

Control signal generator circuit 95 is an identical circuit to that described in the diagram illustrating the conventional control signal generator circuit in Fig.5, but the trigger pulse in this case is the synchronous signal (vertical) of said field signal.

Circuit examples for practically explaining the operation of synthesising selector 93 and control signal selection circuit 14 of synthesiser 9' are as shown in the block diagram of the synthesis selector and control signal selection circuit in the embodiment of the invention in Fig.10.

Where 1st and 2nd segmented data signals are normal in Fig.10, since 1st and 2nd discrimination signals are respectively input as "1", the output of control signal selector circuit 14 is simply the unaltered control signal from the first segmented signal. Thus the output from terminal D of synthesis selector 93 is a synthesised signal with alternating odd- and even-numbered frames as shown in the timing chart (G-1) in Fig.9.

Where the 1st signal is normal and the 2nd abnormal, the 1st discrimination signal input is "1", the 2nd discrimination signal is "0", and the output of control signal selection circuit 14 is "1". Thus the output from terminal D of synthesis selector 93 will be the unaltered input to terminal A of synthesis selector 93 as shown in Fig.9 (G-2), with the result that a synthesised signal in the form of a supplemented 1st segmented data signal is substituted in place of the 2nd segmented data signal, which has been determined to be abnormal.

In the same way, where the 1st signal is abnormal and the 2nd normal, the output of control signal selector circuit 14 is "0", so as shown in Fig.9 (G-3) a synthesised signal is output with a supplemented 2nd segmented data signal substituted for the 1st segmented data signal, which has been determined to be abnormal.

An example of the circuit of received signal selector 15, which samples a clock from segmented data signals in a normal state, is shown in the block diagram for the received signal selector in the embodiment of the invention in Fig.11. In the figure, its output is the 1st segmented data signal where the 1st segmented data signal is normal, but the 2nd segmented data signal is output in the case where the 1st segmented data signal is abnormal and the 2nd segmented data signal is normal, thus ensuring that a normal clock signal output is always obtained from clock sampling circuit 12 in the next step.

As has been described above, it is sufficient that the additional circuits are of simple structure in the case where the number of segments $n = 2$, and the economic value of the application of the invention is particularly great.

Where $n \geq 3$, the possible combination of patterns for segmented signals with abnormalities present and the combination of patterns for the substitute segmented signals which should

replace them is much greater, and, as it is not advisable to expand the logic circuits described above, it is possible to create a receiving end circuit which has the same effect as that described above by recording the corresponding patterns in a ROM and selecting a control signal by reading out from this.

(Effect of the Invention)

As has been described above, where a segmented digital signal exceeds the limit for correction under the error correction encoding method, using the characteristics of television signals the invention synthesises a supplement with a signal having an adjacent field, adjacent line, or adjacent pixel signal with a strong correspondence to the signal, and avoids using a segmented signal with an error or omission,

and, as clock sampling is always carried out on a normal segmented signal,

has a great effect in restoring a television image with low picture deterioration, even in the case where an omission or error has occurred in a data signal in part of the 1-n transmission paths.

4. Brief Description of the Drawings

Fig.1 is a block diagram illustrating the principle of the invention.

Fig.2 is a block diagram illustrating the structure of a conventional circuit at the transmitting end.

Fig.3 is a block diagram illustrating the structure of a conventional circuit at the receiving end.

Fig.4 is a time chart showing data signals for the main parts of a conventional circuit.

Fig.5 is a diagram showing an example of a conventional control signal generator circuit.

Fig.6 is a block diagram showing an example of a conventional segment selector.

Fig.7 is a block diagram which illustrates the circuit structure at the transmission end of an embodiment of the invention.

Fig.8 is a block diagram which illustrates the circuit structure at the receiving end of an embodiment of the invention.

Fig.9 is a time chart for the data signals in the main parts at the receiving end of an embodiment of the invention.

Fig.10 is a block diagram of the synthesis selector and control signal selector circuit in an embodiment of the invention.

Fig.11 is a block diagram of the received signal selector in an embodiment of the invention.

Key to Drawings

1, 1'	A/D converter
2	Band compression encoder
3, 3'	Segmenter
5	Transmitter
6	Clock generator circuit
7, 7'	Receiver
9, 9'	Synthesiser
10	Band compression decoder
11	D/A converter
12	Clock sampling circuit
13,96	Synchronous signal sampling circuit
14	Control signal selector circuit
15	Received signal selector

31,94	Counter
32,95	Control signal generator circuit
33	Segment selector
34,35	Segment FF circuit
41,42,81,82	Buffer memory
71,71',72,72'	Error correction decoder circuit
91,92	Synthesis FF circuit
93	Synthesis selector

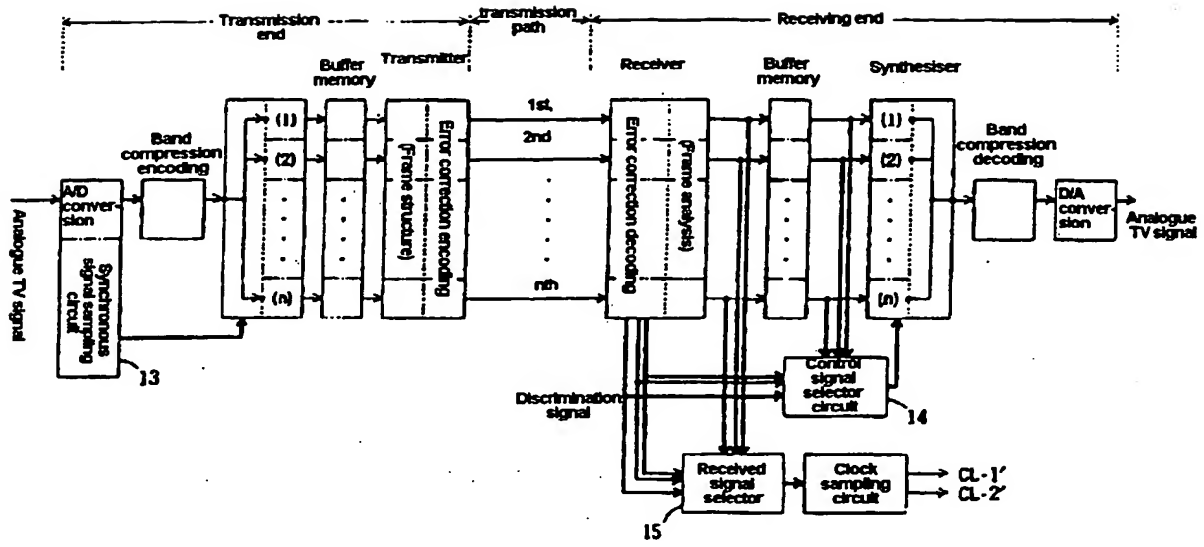

Fig.1: Block diagram illustrating the principle of the invention

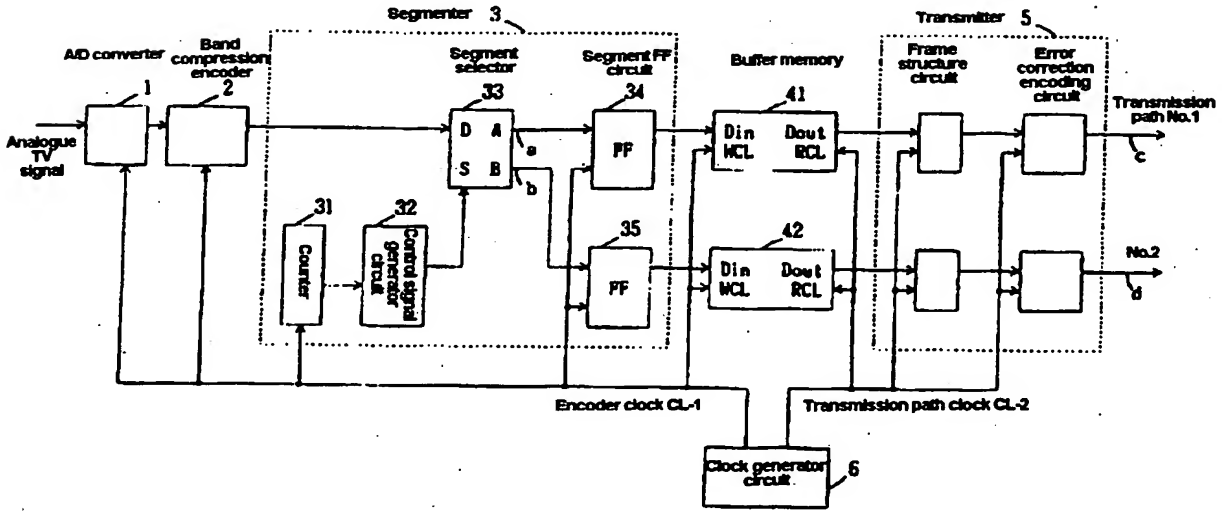

Fig.2: Block diagram illustrating the structure of a conventional circuit at the transmitting end.

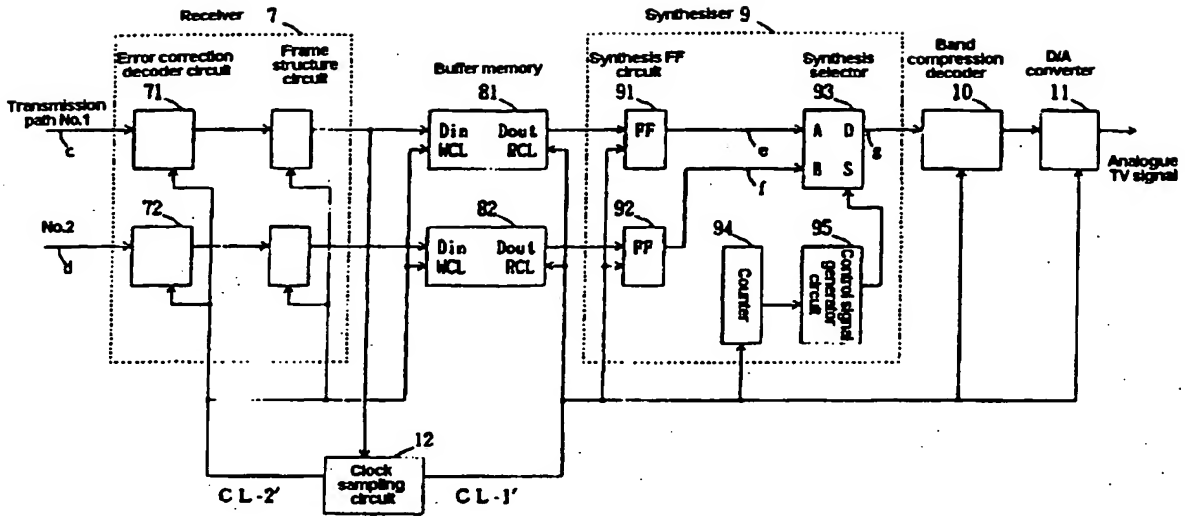

Fig.3: Block diagram illustrating the structure of a conventional circuit at the receiving end.

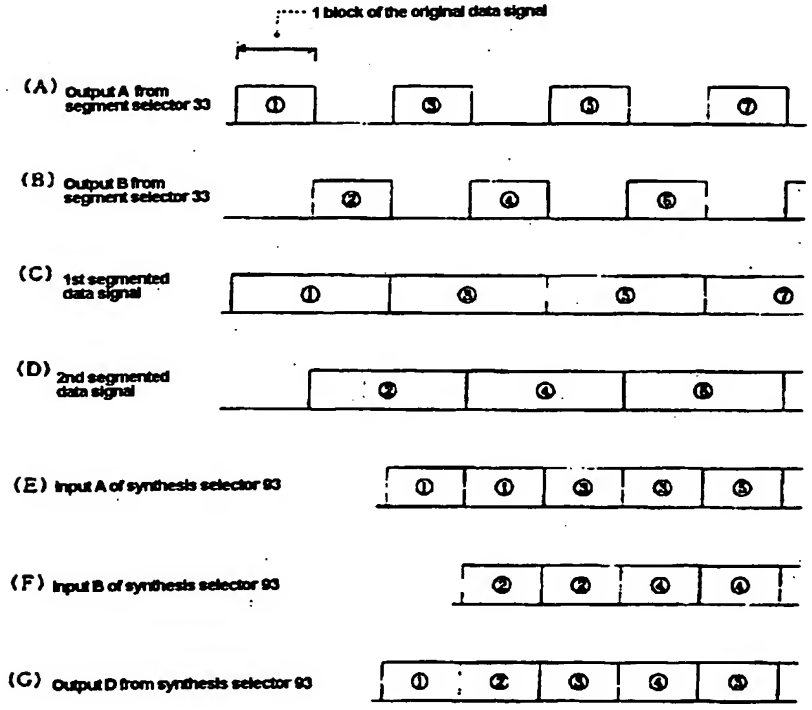

Fig.4: Time chart showing data signals for the main parts of a conventional circuit.

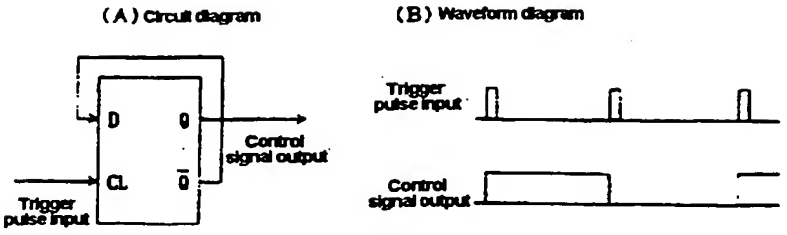

Fig.5: Diagram showing an example of a conventional control signal generator circuit.

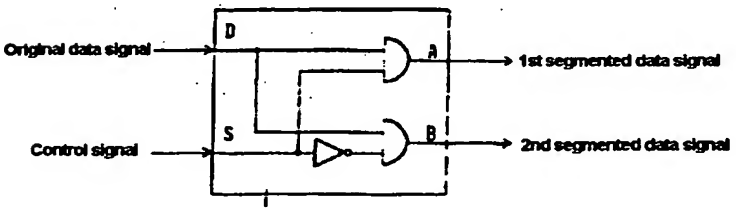

Fig.6: Block diagram showing an example of a conventional segment selector.

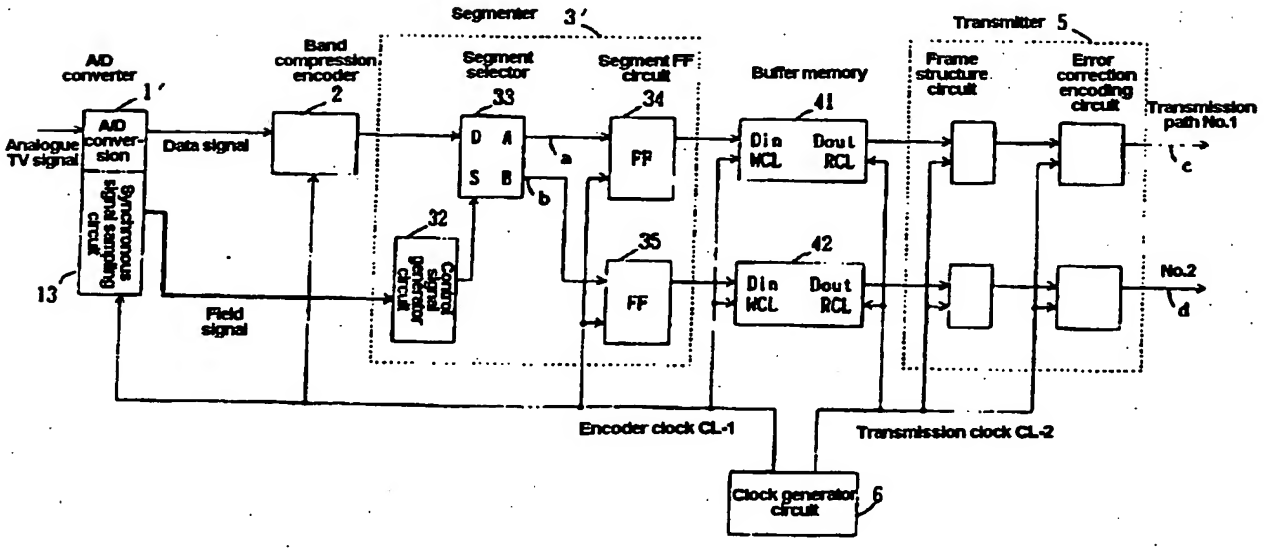

Fig.7: Block diagram illustrating circuit structure at the transmission end of an embodiment of the invention

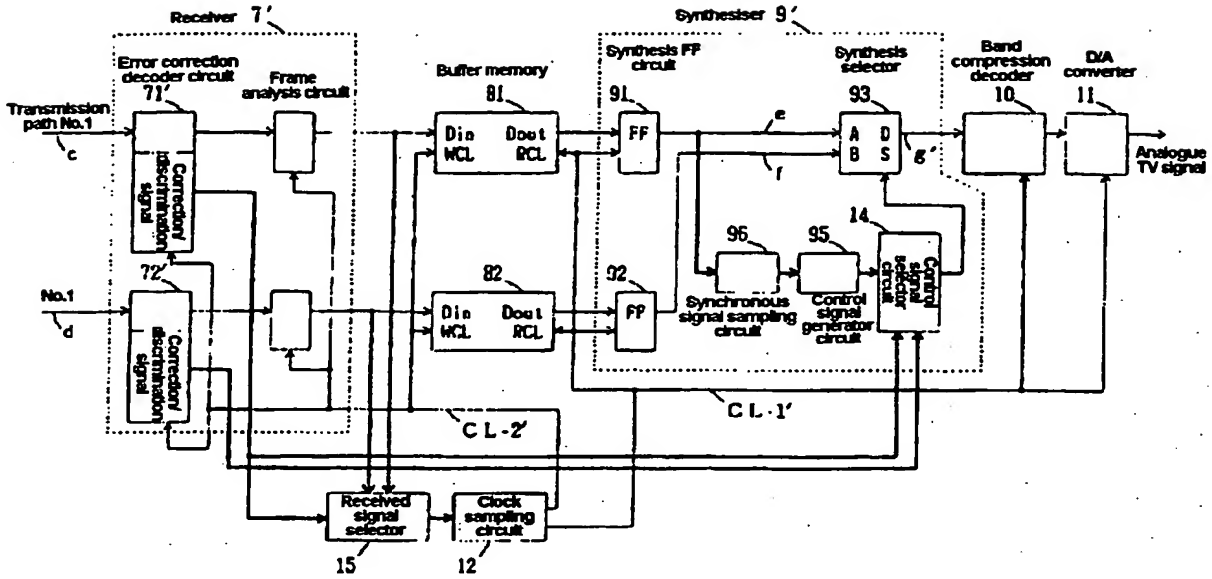

Fig.8: Block diagram illustrating circuit structure at the receiving end of an embodiment of the invention

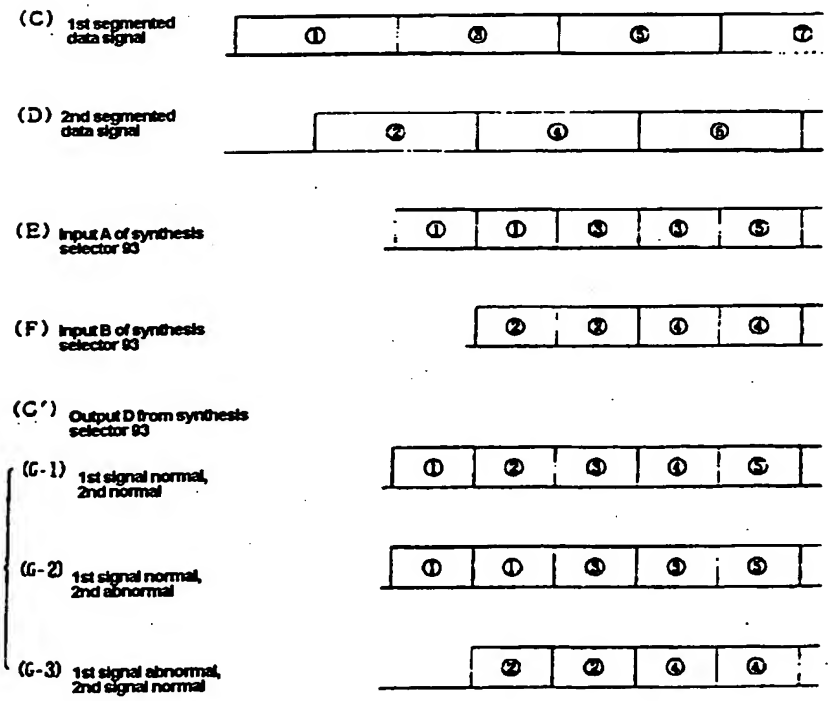

Fig.9 Time chart for data signals in the main parts at the receiving end of an embodiment of the invention

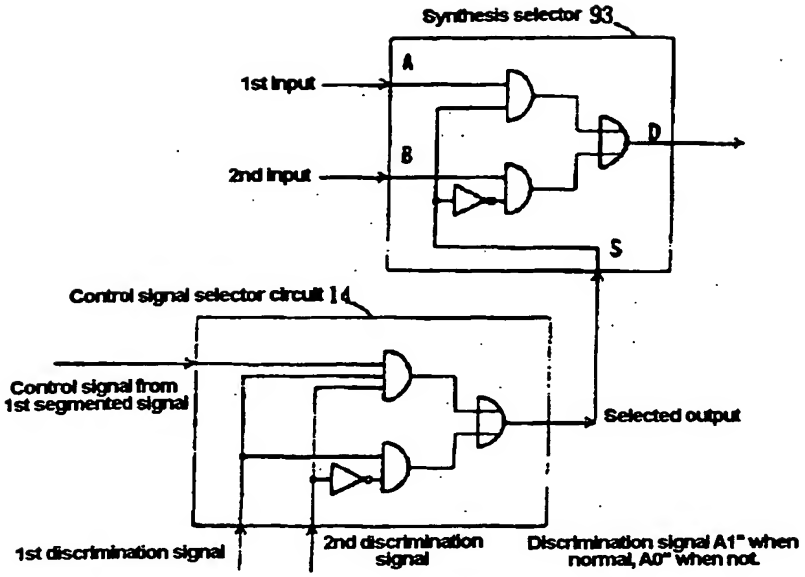

Fig.10: Block diagram of synthesis selector and control signal selector circuit in an embodiment of the invention.

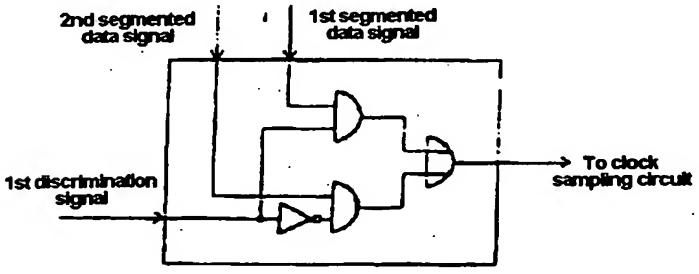

Fig.11: Block diagram of received signal selector in an embodiment of the invention.